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1	BRS	L1	55	interleav\$3 near5 ((u near5 v) or (s near5 t))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 16:20
2	BRS	L2	14	1 and (texture\$1 or texel\$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 16:09
3	BRS	L3	131	interleav\$3 near5 ((address or (x near3 y)) near3 bits)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 16:29
4	BRS	L4	13	3 and 345/\$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 16:40
5	BRS	L5	587	interleav\$3 adj2 bits	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 17:31
6	BRS	L6	21	5 and 345/\$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 16:40
7	BRS	L7	28	5 near5 address	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 16:44
8	BRS	L8	55	(interleav\$3 near2 bits) near3 address\$2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 17:23
9	BRS	L9	29466	zigzag\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 17:24
10	BRS	L10	366	9 same address\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 17:24
11	BRS	L11	0	5 and 10	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 17:25
12	BRS	L12	0	10 and 3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 17:25
13	BRS	L13	17	10 and 345/\$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 17:25
14	BRS	L14	1371	interleav\$3 near1 bit\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 17:33
15	BRS	L15	5	14 and (tile\$1 same linear)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2001/06/03 17:33

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**5 A 128 K\*8 70-MHz multiport video RAM with auto register reload and 8\*4 WRITE feature**

Pinkham, R.; Russell, D.; Balistreri, A.; Herndon, T.H.; Anderson, D.; Mehta, A.; Ngu Hong, N.H.; Sakurai, H.; Hatakoshi, S.; Guillemaud, A.

Solid-State Circuits, IEEE Journal of , Volume: 23 Issue: 5 , Oct. 1988

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**13 Performance of variable rate bit interleaved coding for high bandwidth ef**  
*Lau, V.K.N.*

Vehicular Technology Conference Proceedings, 2000. VTC 2000-Spring Tokyo. 2000 IE  
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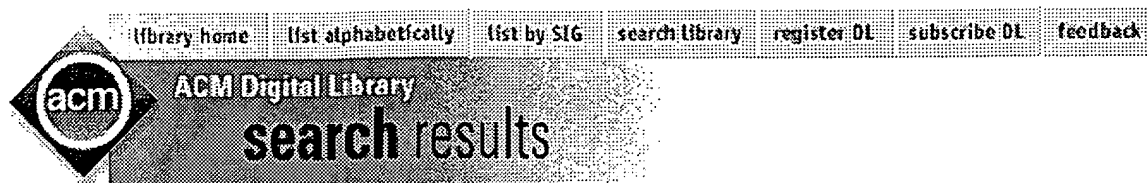
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